*Digital System Design Lab*

# CEL-442



## Lab Journal: 5

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*Class: BCE-6(A).*

### Enrollment no: 01-132182-024

**Implementing Sequential Circuits in Verilog**

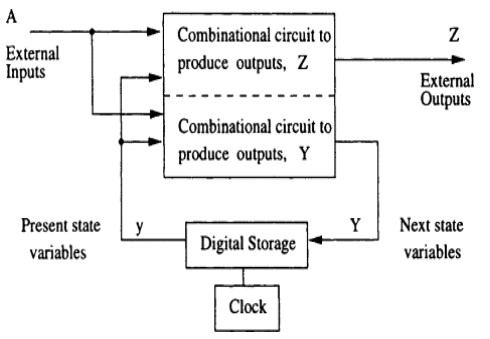
**Objectives:**

* + **To learn and understand the basic concept of Sequential circuits.**
  + **To implement those learnings in the given tasks.**

**Introduction:**

* + **Sequential Circuit:**

The sequential circuit is a special type of circuit that has a series of inputs and outputs. The outputs of the sequential circuits depend on both the combination of present inputs and previous outputs. The previous output is treated as the present state. So, the sequential circuit contains the combinational circuit and its memory storage elements. A sequential circuit does not need to always contain a combinational circuit. So, the sequential circuit can contain only the memory element.



* + **Types:** 
    - ***Asynchronous :***

The clock signals are not used by the Asynchronous sequential circuits. The asynchronous circuit is operated through the pulses. So, the changes in the input can change the state of the circuit. The asynchronous circuits do not use clock pulses. The internal state is changed when the input variable is changed. The un-clocked flip-flops or time-delayed are the memory elements of asynchronous sequential circuits. The asynchronous sequential circuit is similar to the combinational circuits with feedback.

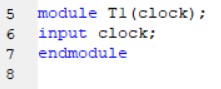
* + - ***Synchronous :***

In synchronous sequential circuits, synchronization of the memory element's state is done by the clock signal. The output is stored in either flip-flops or latches(memory devices). The synchronization of the outputs is done with either only negative edges of the clock signal or only positive edges.

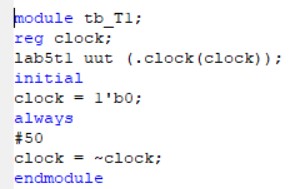
**Tasks:**

* 1. **Generate a clock whose LOW and HIGH TIME changes after every 50-time units.**

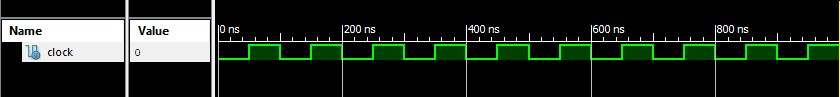
**Module:**



**Stimulus Module:**



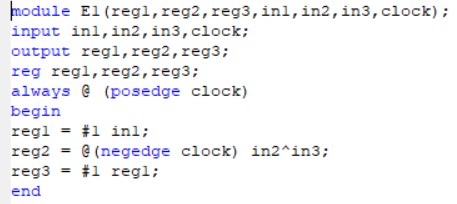
**Output:**



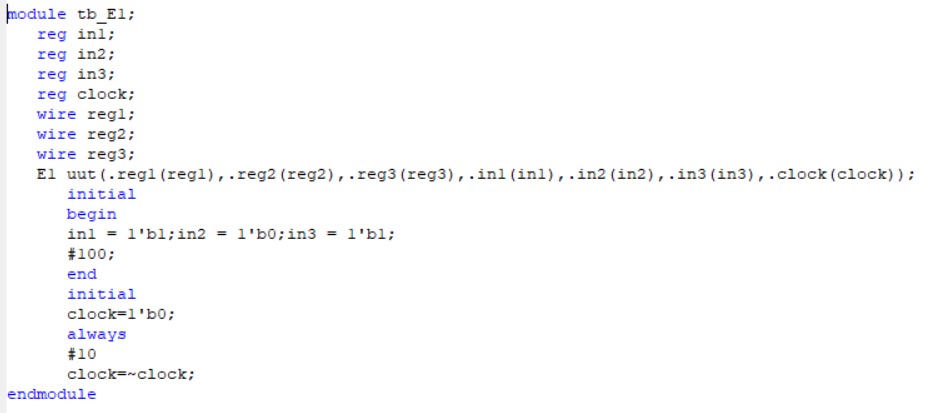
* 1. **Implement all examples one by one.**

**Example 1:**

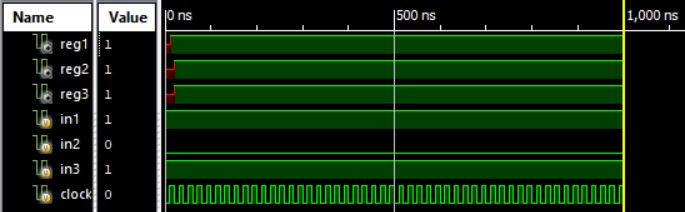
**Module:**



**Stimulus Module:**

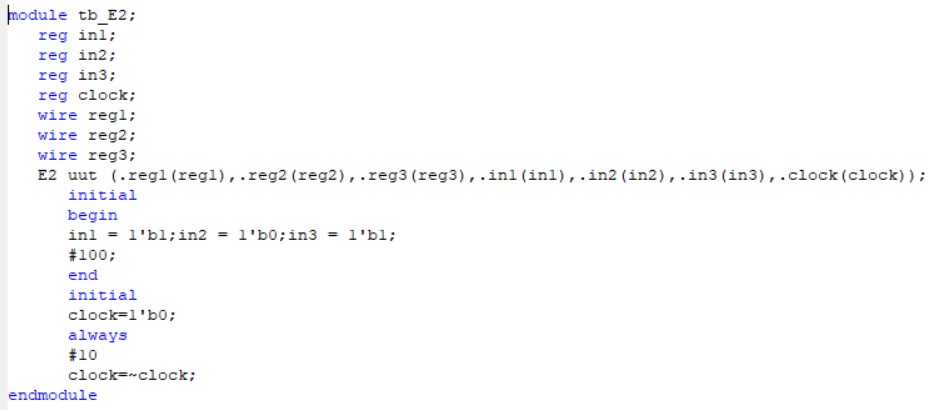
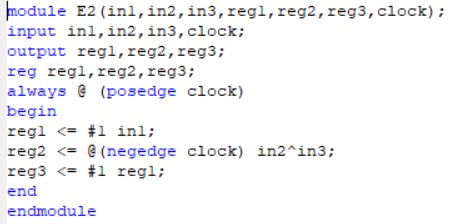


**Output:**

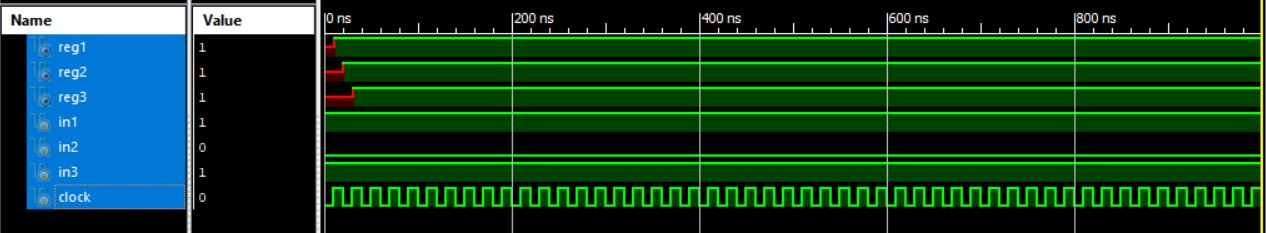


**Example 2:**

**Module:**

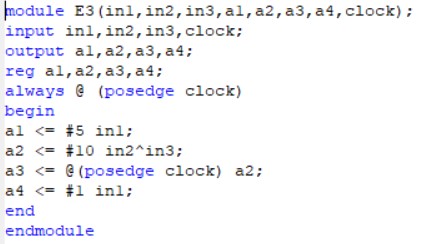


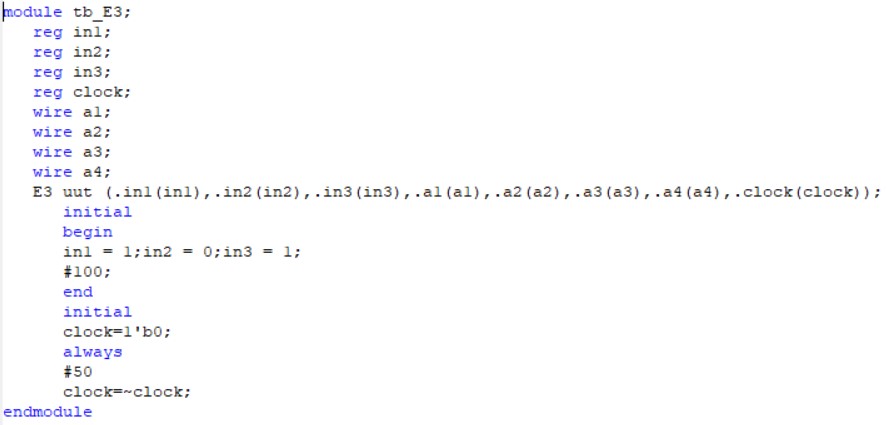
**Output:**



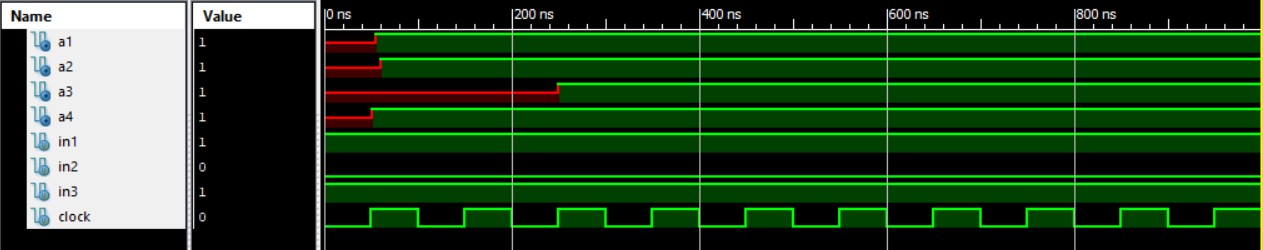
**Example 3:**

**Module:**



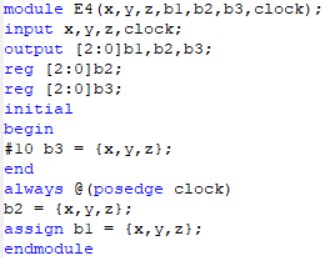


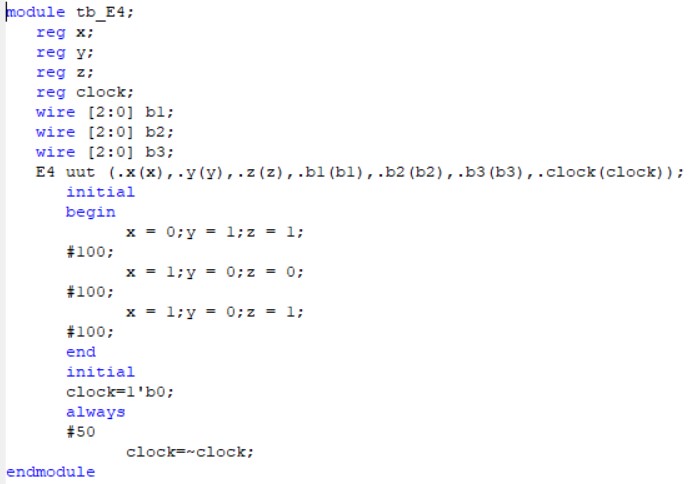
**Output:**



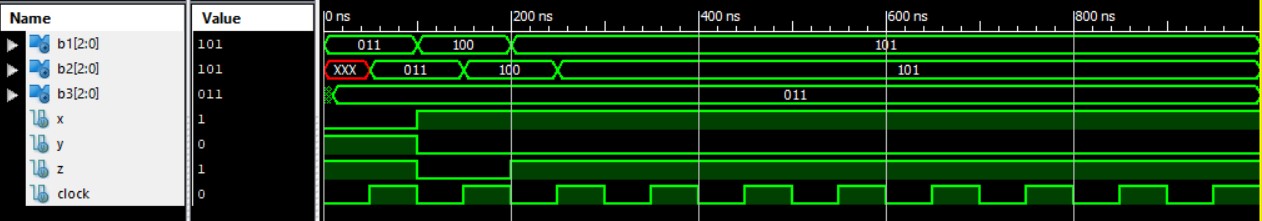
**Example 4:**

**Module:**





**Output:**



**Conclusion:**

*In this lab we learned about* ***Sequential Circuits*** *in Verilog.*